IN THE SPECIFICATION

Please replace the paragraph beginning at line 21, page 1 and ending at line 3, page 2 with the following rewritten paragraph:

As stated above, conventional photolithography techniques may be used to create trenches in the integrated circuit substrate. In photolithography, light may be used to expose a photolithography mask overlying the trench where the light may be reflected off of the integrated circuit layers underneath the mask. The reflections may have detrimental effects on the quality and accuracy of the resulting mask. To improve the results of photolithography at these small scales, SiN (SiON, SiRN) may be used as an anti-reflective coating ~~(ARC)~~ or hard mask layer. The ~~ARC~~ anti-reflective coating layer may reduce or substantially eliminate these reflections thereby resulting in improved masks for creating small features and structures in an integrated device.

Please replace the paragraph beginning at line 5, page 2 with the following rewritten paragraph:

After the formation of the gate, the hard mask/~~ARC~~ anti-reflective coating layer may need to be removed prior to subsequent device processing. The hard mask/~~ARC~~ anti-reflective coating layer may be removed using either a conventional wet strip process or a conventional plasma etching process. A conventional wet strip process may use hot phosphoric acid which may damage the polysilicon layer underlying the ~~ARC~~ anti-reflective coating layer; whereas, a conventional plasma etching process may cause extensive gouging in any exposed field oxide, including in the thermal oxide in an STI region. Gouges in STI regions may alter the isolation properties of the STI region. Further, gouges in STI regions may create an uneven surface causing gap-fill problems for subsequent processing of the device wafer.

Please replace the paragraph beginning at line 15, page 2 with the following rewritten paragraph:

Therefore, there is a need in the art to strip a hard mask/~~ARC~~ anti-reflective coating layer that avoids damage to exposed polysilicon surfaces as well as avoids gouging exposed field oxide such as in STI regions.

Please replace the paragraph beginning at line 2, page 3 with the following rewritten paragraph:

The problems outlined above may at least in part be solved by depositing a protective cap or plug over the hard mask/~~ARC~~ anti-reflective coating layer. The protective cap may be etched back to expose the hard mask/~~ARC~~ anti-reflective coating layer. However, the protective cap still covers and protects the thermal oxide in the trench. By providing a protective cap that covers the thermal oxide in the trench, gouging of the exposed field oxide in STI regions may be avoided.

Please replace the paragraph at line 9, page 3 with the following rewritten paragraph:

In one embodiment of the present invention, a method for avoiding oxide gouging in shallow trench isolation (STI) regions of a semiconductor device may comprise the step of etching a trench in an STI region. The method may further comprise depositing insulating material in the formed trench. The method may further comprise depositing an anti-reflective coating ~~(ARC)~~ layer overlying the STI region and extending beyond the boundaries of the STI region. The method may further comprise etching a portion of the ~~ARC~~ anti-reflective coating layer over the STI region leaving a remaining portion of the ~~ARC~~ anti-reflective coating layer over the STI region and extending beyond the boundaries of the STI region. The method may further comprise depositing a protective cap covering the STI region and extending beyond the boundaries of the STI region. The deposited protective cap covers the remaining portion of the ~~ARC~~ anti-reflective coating layer as well as the insulating material in the trench.

Please replace the paragraph beginning at line 21, page 3 and ending at line 5, page 4 with the following rewritten paragraph:

In another embodiment of the present invention, a device may comprise a trench in a shallow trench isolation (STI) region. The device may further comprise insulating material filled in the trench. The device may further comprise a gate oxide layer covering a portion of the STI region and extending beyond the boundaries of the STI region. The device may further comprise a polysilicon layer overlying the gate oxide layer where the polysilicon layer covers the portion of the STI region and extends beyond the boundaries of the STI region. The device may further comprise an anti-reflective coating ~~(ARC)~~ layer overlying the polysilicon layer where the ~~ARC~~ anti-reflective coating layer covers the portion of the STI region and extends beyond the boundaries of the STI region. The device may further comprise a protective cap overlying the ~~ARC~~ anti-reflective coating layer where the protective cap covers the entire STI region and extends beyond the boundaries of the STI region. Specifically, the protective cap covers the ~~ARC~~ anti-reflective coating layer covering the portion of the STI region and covers the insulating material filled in the trench over the STI region.

Please replace the paragraph beginning at line 11, page 5 with the following rewritten paragraph:

Figures 3A through ~~3F~~ 3G illustrate various stages in the fabrication of an integrated circuit in an STI region of a wafer in accordance with an embodiment of the present invention.

Please replace the paragraph beginning at line 24, page 6 and ending at line 15, page 7 with the following rewritten paragraph:

As stated in the Background Information section, in the fabrication of a semiconductor device using STI techniques, the hard mask/~~ARC~~ anti-reflective coating layer may need to be removed prior to subsequent device processing. The hard mask/~~ARC~~ anti-reflective coating layer may be removed using either a conventional wet strip process or a conventional plasma etching process. A conventional wet strip process may use hot phosphoric acid which may damage the polysilicon layer underlying the ~~ARC~~ anti-reflective coating layer; whereas, a

conventional plasma etching process may cause extensive gouging in any exposed field oxide, including in the thermal oxide in an STI region. Gouges in STI regions may alter the isolation properties of the STI region. Further, gouges in STI regions may create an uneven surface causing gap-fill problems for subsequent processing of the device wafer. Therefore, there is a need in the art to strip a hard mask/~~ARC~~ anti-reflective coating layer that avoids damage to exposed polysilicon surfaces and avoids gauging exposed field oxide such as in STI regions. The hard mask/~~ARC~~ anti-reflective coating layer may be stripped while avoiding gouging the exposed field oxide in the STI regions using the method described below in association with Figures 2 and 3A-F. Figure 2 is a flowchart of a method for avoiding field oxide gouging in shallow trench isolation (STI) regions of a semiconductor device in accordance with an embodiment of the present invention. Figures 3A-F illustrate an embodiment of the present invention of the various stages in the fabrication of an integrated circuit in an STI region of a wafer using the method described in Figure 2. Figures 2 and 3A-F will be discussed in conjunction with one another.

Please replace the paragraph beginning at line 22, page 7 with the following rewritten paragraph:

In step 203, a gate oxide layer 30 is formed over the STI region, e.g., STI region 14, and extends beyond the boundaries of the STI region, e.g., STI region 14, as illustrated in Figure 3A. In step 204, a polysilicon layer 32 is deposited over gate oxide layer 30 as illustrated in Figure 3A. In step 205, an anti-reflective coating ~~(ARC)~~ layer 34 is deposited over polysilicon layer 32 as illustrated in Figure 3A. In step 206, a mask layer 36 is deposited over ~~ARC~~ anti-reflective coating layer 34 as illustrated in Figure 3A.

Please replace the paragraph beginning at line 1, page 8 with the following rewritten paragraph:

In step 207, mask layer 36 and ~~ARC~~ anti-reflective coating layer 34 are patterned and etched over a portion of the STI region, e.g., STI region 14, to expose selected portions of polysilicon layer 32 as illustrated in Figure 3B.

Please replace the paragraph beginning at line 11, page 8 with the following rewritten paragraph:

The remaining ARC layer 34 over the STI region and extending beyond the boundaries of the STI region, e.g., STI region 14, needs to be stripped. As stated above, ~~ARC~~ anti-reflective coating layer 34 needs to be stripped in such a manner as to avoid field oxide gouging. Gouging of the field oxide may be avoided by depositing a protective cap or plug 38, e.g., thin layer of photoresist, in step 210, over the STI region, e.g., STI region 14, and extending beyond the boundaries of the STI region, e.g., STI region 14, as illustrated in Figure 3E. In this manner, the remaining portion of ~~ARC~~ anti-reflective coating layer 34 as well as insulating material 18 is covered by protective cap 38 as illustrated in Figure 3E.

Please replace the paragraph beginning at line 20, page 8 with the following rewritten paragraph:

In step 211, protective cap 38 is etched back to expose ~~ARC~~ anti-reflective coating layer 34 but maintains protection of insulating material 18 as illustrated in Figure 3F. That is, protective cap 38 is etched back to expose ~~ARC~~ anti-reflective coating layer 34 but remains covering insulating material 18 to protect insulating material 18 from etching. In one embodiment, protective cap 38 is a photoresist that is relatively resistant to the types of etching used to remove ~~ARC~~ anti-reflective coating layer 34 from wafer 10. For example, protective cap 38 may be a layer of photoresist with a thickness of about 800 to 1200 Å (Angstroms). In one embodiment, protective cap 38 may be a layer of photoresist with a thickness of about 1000 Å.

Please replace the paragraph beginning at line 1, page 9 with the following rewritten paragraph:

In step 212, ~~ARC~~ anti-reflective coating layer 34 is etched using plasma etching while avoiding gouging of insulating material 18 due to protective cap 38 covering insulating material 18 as illustrated in Figure 3G. It is noted that other

etching techniques besides plasma etching may be used to remove ~~ARC~~ anti-reflective coating layer 34 that is highly selective for removing ~~ARC~~ anti-reflective coating layer 34 and not reactive with the material of protective cap 38. For example, a plasma etching process using CF4, CHF3 and CH3F as the active species may be sufficiently selective to remove ~~ARC~~ anti-reflective coating layer 34 without removing the photoresist used as protective cap 38.